Winbond
ACPI-STR Controller
W83305S
W83305G

W83305S

Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1		Apr./06	0.5	N.A.	All version before 0.5 are for internal use only

LIFE SUPPORT APPLICATIONS

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Table of Contents-

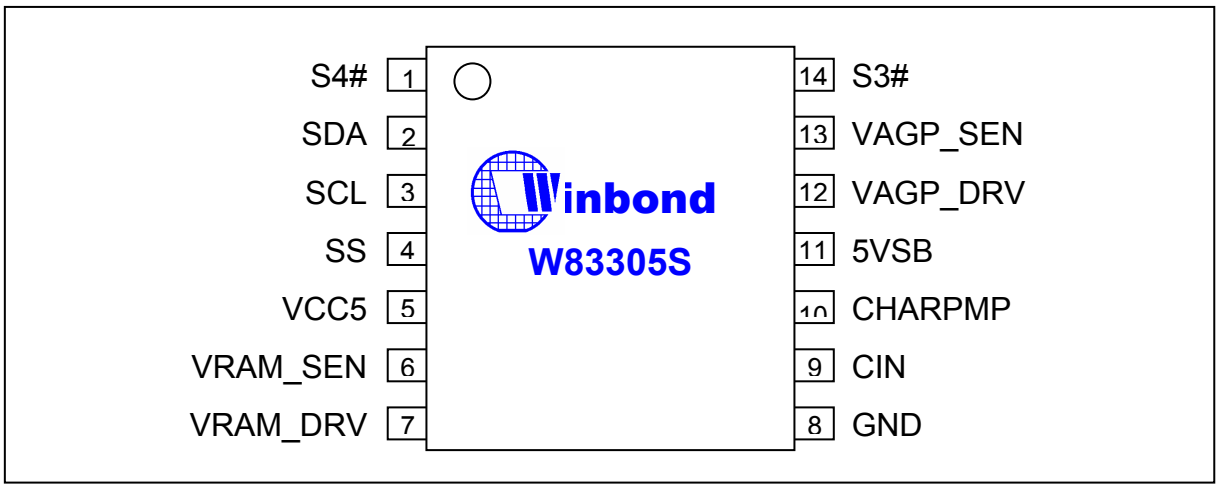
1. GENERAL DESCRIPTION

W83305S is a new power management IC which compliant ACPI specification 2.0 for desktop PC and motherboard. The chip regulates two most voltage-relative powers for DDR SDRAM and AGP slot applications. As the two devices on board, a stable, reliable, and programmable power should be performed for higher reliability, stability, compatibility and better-performance for diverse combination of devices (RAM module and AGP card). The chip is operated basing on a simple dual-wire bus SMBus. Via SMBus control, the power for DDR SDRAM can be adjusted ranging from 2.50V to 3.00V; and the power for AGP slot can be adjusted ranging from 1.50V to 2.00V with 50mV/step. Besides for safety consideration, linear under voltage and soft-start are applied on the two regulated powers. With design of W83305S, a **cost-effective**, **sample, modular, stable, reliable, flexible** and **high-performance** power solution is provides for the motherboard and desktop PC design.

2. FEATURES

- Provides ACPI-Compliant Voltages
  - Programmable 2.55V_{STR} Power for DDR SDRAM
  - Programmable 1.55V_{CC} Power for AGP Slot
- I2C Interface
- Internal Charge Pump Support Voltage Up to 9.5V
- Drive All N-Channel MOSFET
- Soft Start
- Under-Voltage Protection for VAGP, VRAM
- Small footprint package 14-SOP 150mil

3. PIN CONFIGURATION



4. PIN DESCRIPTION

NO	NAME	I/O	FUNCTION DESCRIPTION
1	S4#	I_{ST}	ACPI control signal.
2	SDA	I/O	I2C Interface Pins. The address is defined as 5EH (0101 111X), and X is used to control read/write.
3	SCL	I	
4	SS	I	Soft-Start Pin. Attach an external capacitor (0.1u) on this pin to adjust the soft-start slope-rate.
5	VCC5	I_{ST}	Power VCC5 Input.
6	VRAM_SEN	I	Linear Regulator for DDR SDRAM.
7	VRAM_DRV	O	
8	GND	P	Power Ground.
9	C_{IN}	I	Charge Pump Pins. It supports 5mA driving current and insures output voltage 10V or above.
10	CHRPMP	P	
11	5VSB	P	Power Pin.
12	VAGP_DRV	O	Linear Regulator for AGP slot.
13	VAGP_SEN	I	
14	S3#	I_{ST}	ACPI Control Signal.

5. REGISTER DESCRIPTION

5.1 CR01 (VAGP Over-clocking Configuration Register, Default 0x00h, Read/Write)

BIT0	BIT1	BIT2	V_{AGP} OUTPUT (V)
0	0	0	1.55
0	0	1	1.50
0	1	0	1.60
0	1	1	1.65
1	0	0	1.70
1	0	1	1.80
1	1	0	1.90
1	1	1	2.00

5.2 CR02 (VRAM Over-clocking Configuration Register, Default 0x00h, Read/Write)

BIT0	BIT1	BIT2	V_{RAM} OUTPUT (V)
0	0	0	2.55
0	0	1	2.50
0	1	0	2.60
0	1	1	2.65
1	0	0	2.70
1	0	1	2.80
1	1	0	2.90
1	1	1	3.00

CR03 (Linear Under Voltage Enable/Disable Register, Default 0x03h, Read/Write)

Bit1: Linear under voltage protection enable/disable bit for V_{AGP}

0: Disable 1: Enable

Bit0: Linear under voltage protection enable/disable bit for V_{RAM}

0: disable 1: Enable

5.3 Index 4Ch - Winbond Vendor ID (Low Byte)

Power-on default [7:0] = 1010, 0011 b (A3h)

BIT	NAME	READ/WRITE	DESCRIPTION
7:0	VIDL[7:0]	Read Only	**Vendor ID Low Byte.** Default A3h.

5.4 Index 4Dh - Winbond Vendor ID (High Byte)

Power-on default [7:0] = 0101, 1100 b (5Ch)

BIT	NAME	READ/WRITE	DESCRIPTION
7:0	VIDH[7:0]	Read Only	**Vendor ID High Byte.** Default 5Ch

5.5 Chip ID -- Index 4Eh

Power on default [7:0] = 1010, 0000 b

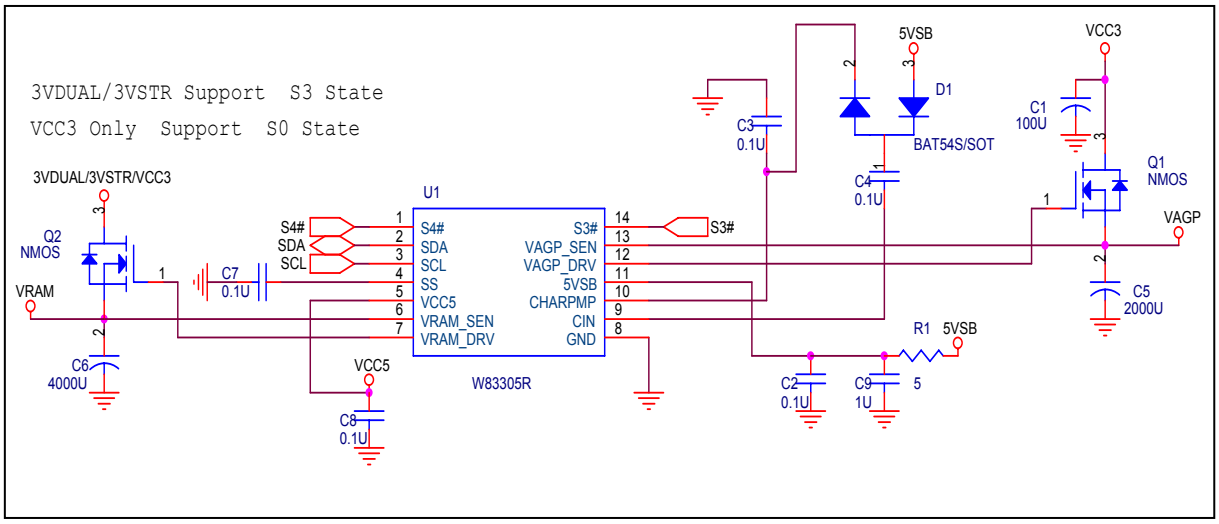
BIT	NAME	READ/WRITE	DESCRIPTION
7-0	CHIPID[7:0]	Read Only	**Winbond Chip ID number.** Read this register will return 0xa0h for W83305S.

5.6 Reversion ID -- Index 4Fh

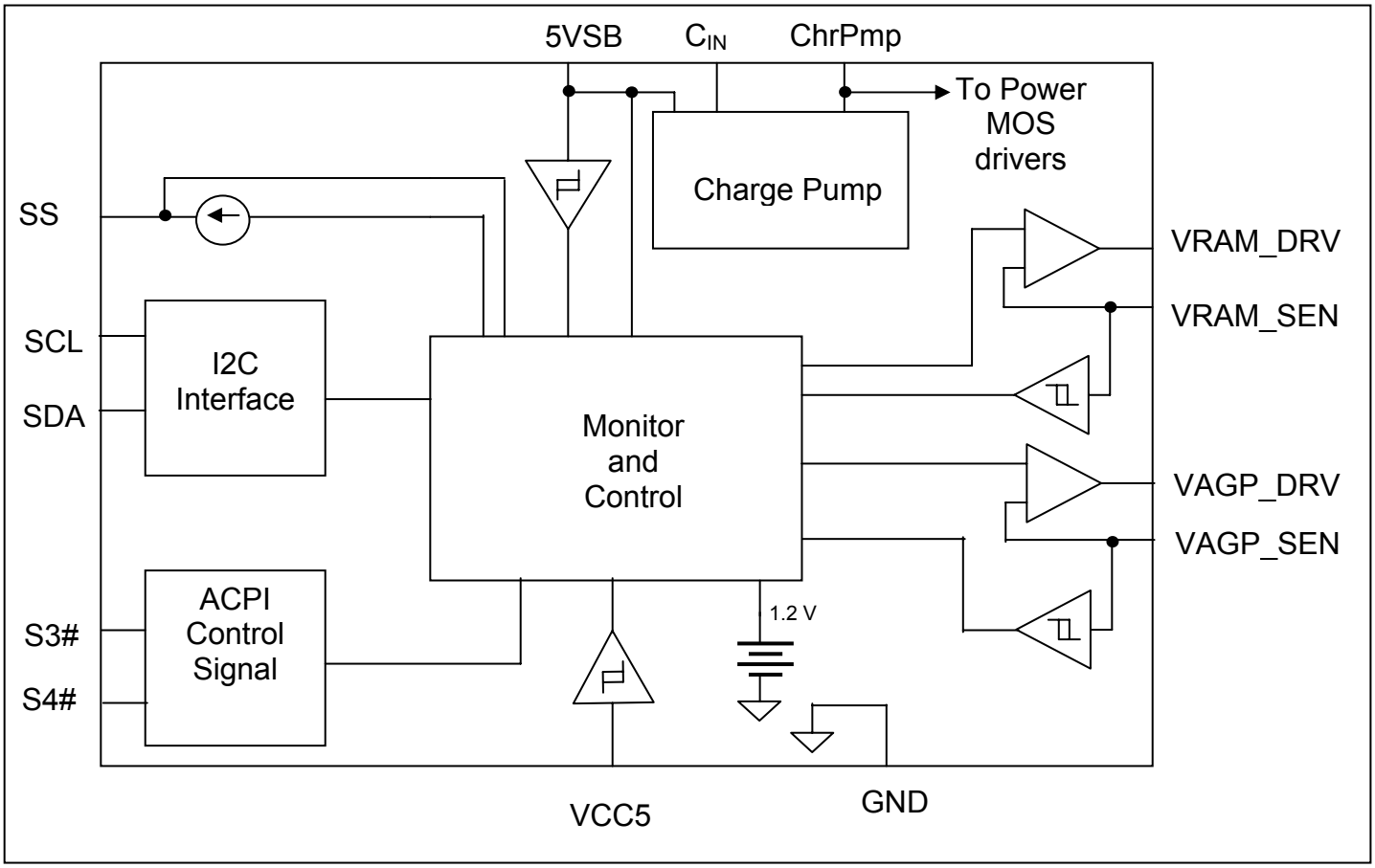
Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	CHIPID[7:0]	Read Only	**Winbond Chip ID number.** Read this register will return 0x00h for W83305S.

6. APPLICATION CIRCUIT



7. INTERNAL BLOCK DIAGRAM



8. ELECTRICAL CHARACTERISTICS

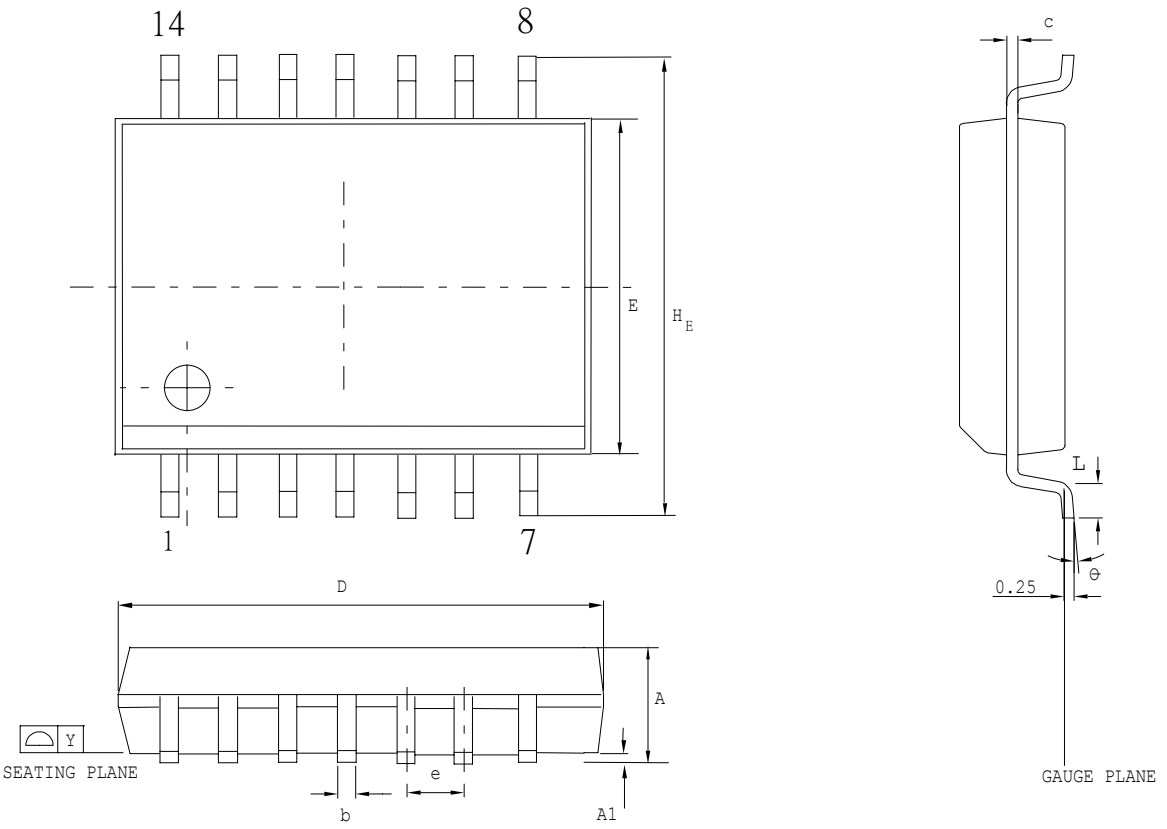
AC Characteristics

VCC=5V ± 5 %, T_A = 0°C TO +70°C						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
VAGP REGULATOR 0						
Nominal Output Voltage			1.55		V	CR01(bit0,bit1,bit2)=000
Nominal Output Voltage			1.50		V	CR01(bit0,bit1,bit2)=001
Nominal Output Voltage			1.60		V	CR01(bit0,bit1,bit2)=010
Nominal Output Voltage			1.65		V	CR01(bit0,bit1,bit2)=011
Nominal Output Voltage			1.70		V	CR01(bit0,bit1,bit2)=100
Nominal Output Voltage			1.80		V	CR01(bit0,bit1,bit2)=101
Nominal Output Voltage			1.90		V	CR01(bit0,bit1,bit2)=110
Nominal Output Voltage			2.00		V	CR01(bit0,bit1,bit2)=111
Regulation				5	%	
Under-Voltage Falling Threshold			73.3 %		%	
VAGP_DRV Output Voltage		8			V	CR0F=80h I(VAGP_DRV) < 0.1mA
VRAM2.5 REGULATOR						
Nominal Output Voltage			2.55		V	CR02(bit0,bit1,bit2)=000
Nominal Output Voltage			2.50		V	CR02(bit0,bit1,bit2)=001
Nominal Output Voltage			2.60		V	CR02(bit0,bit1,bit2)=010
Nominal Output Voltage			2.65		V	CR02(bit0,bit1,bit2)=011
Nominal Output Voltage			2.70		V	CR02(bit0,bit1,bit2)=100
Nominal Output Voltage			2.80		V	CR02(bit0,bit1,bit2)=101
Nominal Output Voltage			2.90		V	CR02(bit0,bit1,bit2)=110
Nominal Output Voltage			3.00		V	CR02(bit0,bit1,bit2)=111
Regulation				5	%	
Under-Voltage Falling Threshold			76%		%	
MAX VRAM_2.5_DRV Output Voltage		8			V	I(VRAM_2.5_DRV) < 0.1mA

CHARGE PUMP						
Charge Pump Frequency		160	200	240	KHz	
Charge Pump Voltage		9.2	9.5			

LOGIC LEVEL		HIGH	LOW
S3	2.55±0.3V	2.55±0.3V	
S4	2.55±0.3V	2.55±0.3V	

9. PACKAGE SPECIFICATION



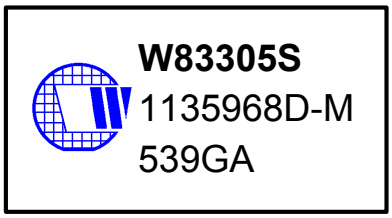
Control demensions are in milmeters .

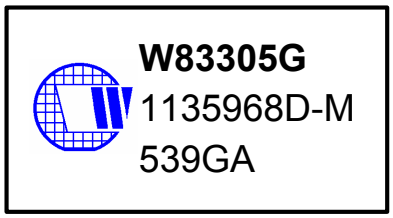
SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	8.55	8.75	0.337	0.344
e	1.27 BSC		0.050 BSC	
H_E	5.80	6.20	0.228	0.244
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

10. ORDERING INFORMATION

PART NO.	PACKAGE	REMARKS
W83305S	14-SSOP	Operation - Commercial 0~70℃
W83305G	14 SSOP	Operation - Commercial 0~70℃ PB-free package

11. HOW TO READ THE TOP MARKING





Left Line: Winbond Logo

1st Line: IC Part No - W83305S,W83305G(Pb-free package)

2nd Line: IC Lot No – XXXXXXXX

3rd Line: Assembly Date (X: Assembly Year + XX: Assembly Week) + Assembly House Code (G- GR; O- OSE; A- ASE, etc…) + IC Version (X)

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